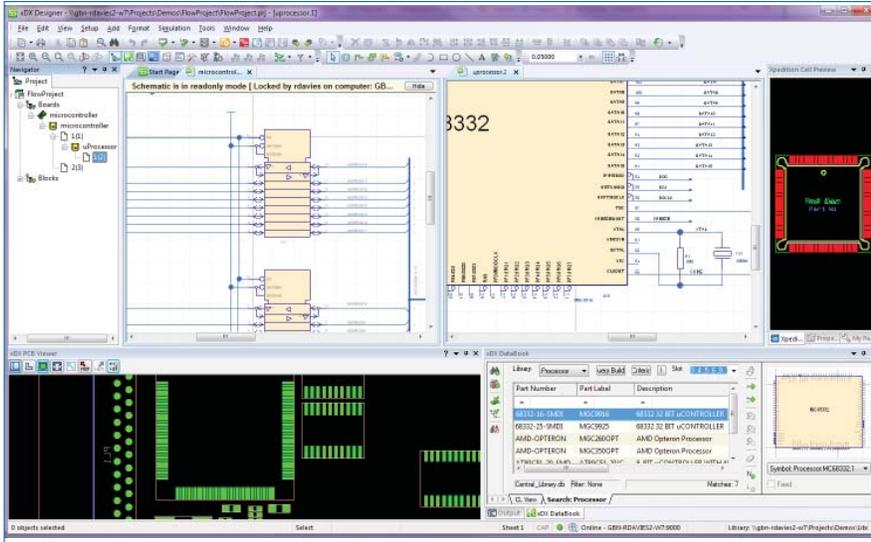


Schematic/Design Creation



xpeditio xDX Designer is a complete solution for design creation, definition, and reuse.

Overview

Creating competitive products is about more than capturing a schematic and passing the design to layout. Libraries must be managed so that the optimal parts with the lowest cost and shortest lead-time are used in the design.

Sections of designs must be reused to reduce development time and improve reliability. Simulation and signal integrity analysis must be performed to ensure that the design will function properly and can be manufactured. Constraints must be applied early in the process so that fewer design iterations are required. Finally, the design data must be distributed and integrated with the purchasing and manufacturing operations so that a complete product can be produced with the fewest errors in the least amount of time.

xpeditio[®] xDX Designer provides a complete solution for design creation, definition, and reuse. It provides everything needed for circuit design and simulation, component selection, library management and signal integrity planning in a concurrent team-based design environment.

Powerful Features for High Productivity

Designed to support the most complex designs yet be easy to use, the schematic editor provides the designer with unparalleled design capabilities including multiple levels of hierarchy and an unlimited number of schematic sheets.

To improve your design team's productivity, real-time concurrent design entry by multiple designers working on the same data set is supported. Addressing the needs of both seasoned veterans and casual users the interface is designed to help you get the job done in the minimum of time. Fully contextually aware, the editor provides only the information needed by the user to get the current task completed, allowing you to concentrate on the design task in hand.

MAJOR BENEFITS:

- Concurrent team design environment shortens design time
- Intelligent hierarchical support for true design reuse saves time
- Simplified entry of physical and electrical constraints with integrated constraint editor
- Integrated library browser for intuitive parts management
- Integrated variant manager simplifies design variant support
- Integrated interconnect editor for table-based design of high pin-out components eliminates errors
- Single tool for digital, RF, Analog, and mixed signal design and simulation support for ease of use
- HyperLynx Signal and Power Integrity tools can be run from inside, greatly simplifying use
- Use with Mentor PCB and other 3rd party PCB layout packages

Interactive tool tips provide additional information to the user when required, enabling new users to get up to speed quickly.

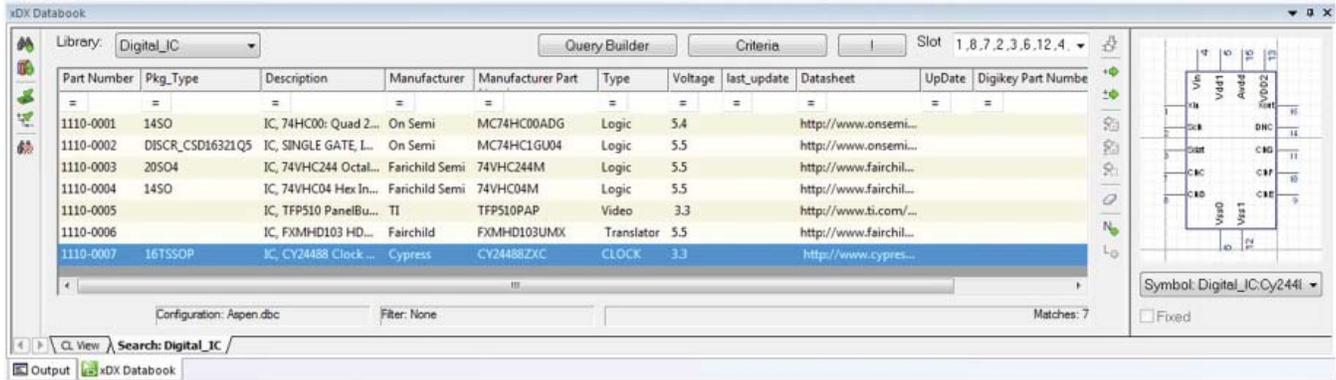
Using design templates, the system can be pre-configured to support multiple different project setups to suit your design teams. Templates include settings for the Part library, sheet size and sheet border, specialized pins for block input and output, power and ground, and on and off sheet connectors. The use of templates ensures users are productive immediately they start a new design. Additional features are designed to improve the user's productivity.

The schematic design tool can be configured to support your specific design needs by adding optional components. Additional components include the component information system for centralized library access, export to PDF for documentation, variant design

cycle, causing costly redesigns or quality problems. Component information can come from a variety of sources including corporate parts databases, manufacturers' data books and design systems. When adding component information to the design, outdated and missing data can affect design integrity and manufacturability. A more reliable solution is to have all the latest information accessible to all designers throughout the enterprise.

Simplified Library Management

Integrated with the Xpedition xDM Library for the logical symbol view and physical part view, Xpedition xDX Databook allows the designer to search the corporate data directly within the schematic editor, enabling design engineers to quickly search for and locate parts over a corporate intranet or the Internet



The xDX Databook allows searching corporate data from within the schematic editor.

definition, formal design re-use, integration to RF and high speed analysis tools and additional PCB interfaces to support alternative PCB layout systems.

Finally, an open object model provides complete access to data and commands through standard VBScript or JScript languages, allowing for extensive customization.

Component Information Management

For the electronic engineer developing a product, the ability to manage and quickly access corporate component information is critical to success. But geographically dispersed design teams often use separate component databases, which may be out of sync or out of date. This can cause mistakes during product development that go undetected until later in the design

xDX Databook

Using the Xpedition Central Library as the source of the logical and physical PCB data ensures a correct-by-design implementation within the printed circuit board while minimizing data duplication in the library. By connecting to an external source for part characterization, the component information manager enables additional manufacturing data to be annotated to each component ensuring the part can be purchased to your company specifications and cost restrictions.

Accessing Library Data

The component information manager can connect to any ODBC-compliant database, including Mentor Graphics xDM Library Server. Alternatively the component information management system may be connected to

other databases that provide the parametric data needed to uniquely identify and procure parts for your PCBs, including Microsoft Access, Oracle and SQL Server.

Typical Product Usage

The designer can use the component information manager to search for part information in the library, and with the use of sophisticated filters can narrow down the parts to use in the design based on any of the data fields in the database. The library data source may also provide access to data sheets, detailed physical layout data and, when connected to xDM Library Server, information about which other designs use a particular component. Parts can then be added to the design directly from the search results in the spread sheet like interface.

The designer can also add a generic component to a schematic. For example, an engineer may want to postpone selecting a part's package style or value until he has completed further analysis. When it is time to order the part, the designer can select the component and run a verification pass on it, the component information manager then automatically displays the available parts with matching characteristics and highlights the missing information. The engineer can then select the required part and annotate the missing information to the generic component.

Alternatively, the user can verify the integrity of the entire design from within the component information manager, ensuring that the information on the schematic is consistent with the data required for procurement and manufacture and automatically annotating any missing attribute information.

The tool also provides access to design reuse blocks that have been stored in the corporate library. The same search capabilities can be used to search for a specific reuse block, or for reuse blocks that meet a set of criteria. This makes it easy to find the right reusable design for incorporation in a new schematic.

Design Reuse

Design reuse is a method of reducing development costs, design time and potentially manufacturing costs by reusing your intellectual property (IP) in a controlled environment, thus minimizing the variety of components held in stock. The design reuse process

also encourages design best practice while increasing product functionality and reliability.

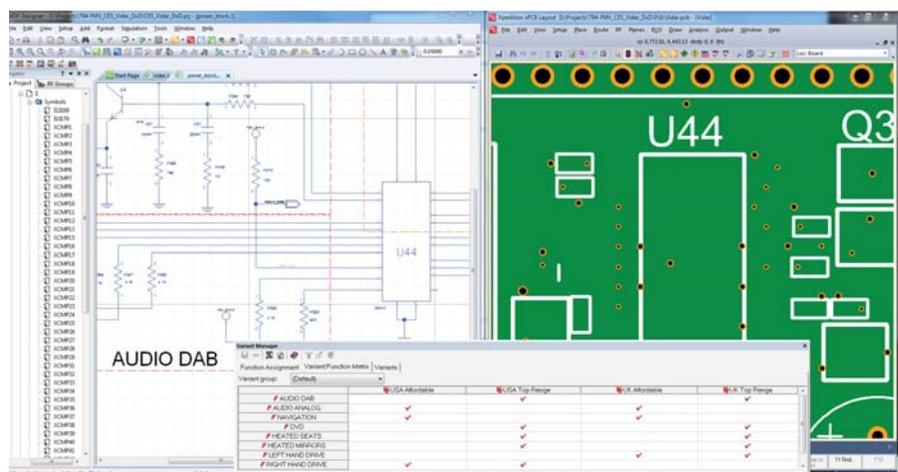
A reusable design is managed in the library as a certified circuit and may consist of just a schematic (logical reuse) or a complete function comprising schematic, PCB layout and constraints (logical-physical reuse).

Full support for hierarchy in the schematic editor allows for multiple instantiations of the reuse block within the design. Usually added as a 'read-only' schematic to prevent changes to the design performance, the editor includes the ability to dissolve the schematic instance of the reuse block removing the read only status allowing edits; without affecting the source design stored in the library, or other instances of the block in the host design. To support design documentation specialized attributes limit the repackaging of components within the reuse block by adding a unique prefix/suffix to all of the components in the re-use circuit block.

Variant Management

Design variants based on a common PCB layout is another form of design reuse supported by the schematic tools.

A common integrated variant manager interface, shared with both the schematic and layout tools, provides an easy to use environment for defining the content of each variant of a design. Each variant is stored within the design project as a separate view with the benefit that whenever the master design is updated with changes each variant view is updated automatically, thus reducing the required work and maintenance of design data.



Integrated Common Variant Interface for Schematic and Layout.

Both physical and functional variants are supported. Physical variants are based on the actual layout of the PCB and include options to substitute or exclude parts. Functional variants are based on the logical design and allow for complete sections of logic to be excluded irrespective of physical placement.

A component (or block) can be marked for exclusion using 'DO NOT FIT' or substituted for a different component from the corporate component database whilst maintaining the integrity of the board layout by using a user specified characteristic such as the PCB footprint.

Once all variant views have been defined the documentation for each variant can be produced as an intelligent PDF document of the variant schematic, a Bill-Of-Materials and a Parts List.

Constraint Based Design

Rules to manage the manufacturing standards of the board and the routing of high speed signals to meet the performance requirements of the board are fundamental to the success of the final board assembly.

The Constraint Manager spreadsheet is extremely flexible, allowing the assignment of rules and constraints to a large variety of design elements and provides a common, integrated constraint definition environment for both schematic capture and layout.

xDX Designer's Integrated Constraint Manager

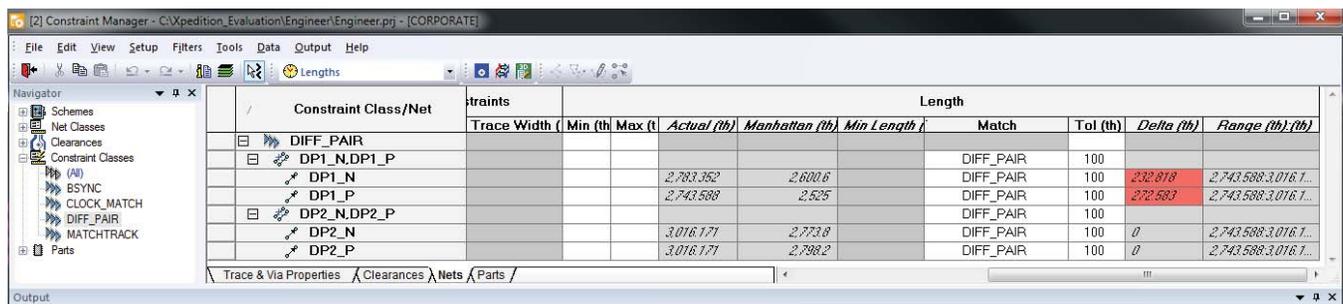
The integrated Constraint Editor is an easy to use constraint view of the electrical nets under edit. In the view above the four nets selected are displayed in the constraint editor as differential pair electrical nets

These physical and electrical constraints can be read directly by HyperLynx Signal and Power Integrity analysis tools. Once analysis is complete, these constraints are automatically passed to the Xpedition PCB layout system where the user is alerted to changes in connectivity and constraint data by a traffic light early warning display.

LineSim Integration into HyperLynx

The LineSimLink integration with HyperLynx allows you to create a Virtual Prototype of your PCB design for signal integrity analysis and also validate your board characteristics from the xDX Designer cockpit. For design exploration purposes designers can select, review and change the board characteristics for the simulation and analysis of their virtual prototype directly from within the HyperLynx Stackup Editor.

This intuitive fully featured design and analysis environment provides a high-quality signal integrity analysis environment that is not only easy to use and easy to access via LineSim Link, and is therefore ideal for new or



Constraint Class/Net	Constraints		Length							
	Trace Width (th)	Min (th)	Max (t)	Actual (th)	Manhattan (th)	Min Length (th)	Match	Tol (th)	Delta (th)	Range (th): (th)
DIFF_PAIR										
DP1_N, DP1_P				2,783.352	2,600.6		DIFF_PAIR	100		
DP1_N				2,743.588	2,525		DIFF_PAIR	100	232.818	2,743.588:3,016.1...
DP1_P							DIFF_PAIR	100	272.583	2,743.588:3,016.1...
DP2_N, DP2_P							DIFF_PAIR	100		
DP2_N				3,016.171	2,773.8		DIFF_PAIR	100	0	2,743.588:3,016.1...
DP2_P				3,016.171	2,788.2		DIFF_PAIR	100	0	2,743.588:3,016.1...

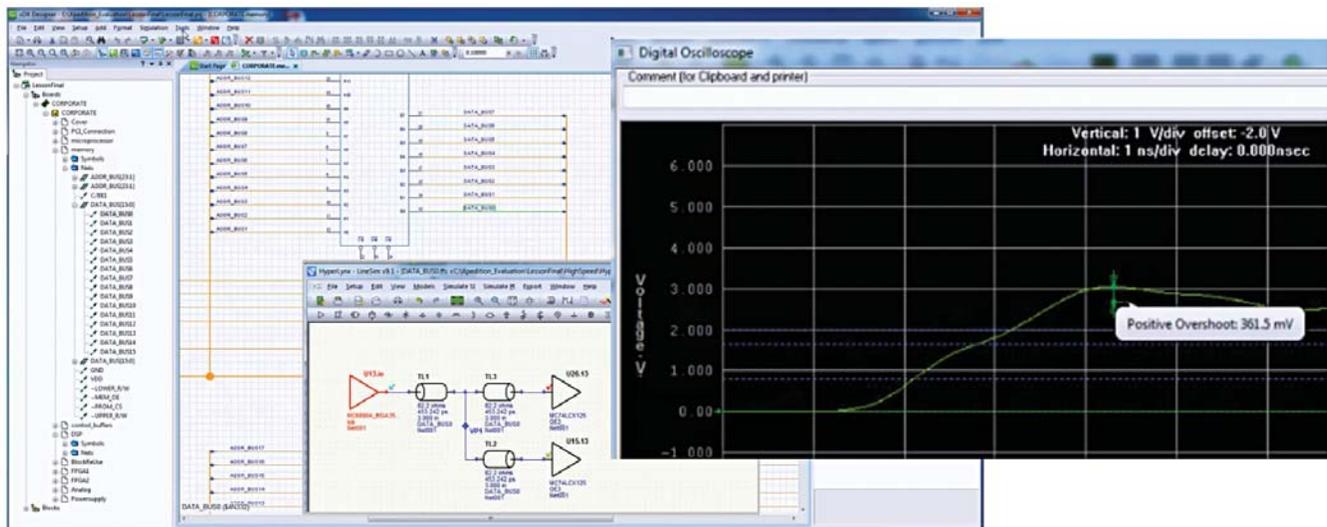
Constraints Manager Integrated common definition with schematic and layout.

The Constraint Manager supports definition and verification of electrical and physical constraints within one environment, simplifying a complex constraint entry process while improving design accuracy.

Later in the design process the actual routed trace can be verified against the initial constraint definition, directly from within the Constraint Manager environment, here highlighted in red, indicating the difference between the defined rule and the actual routed net

casual users, but is powerful enough for the domain expert. All from a single cockpit for logical design and simulation

Sometimes to address issues such as Signal Integrity overshoot problems shown in the LineSim digital oscilloscope, designers will need to add some termination to the automatically generated transmission line model.



xDX Designer with LineSim.

RC Termination is easily added to the schematic by a simple drag and drop of the resistor at the transmission line output. Rather than trial and error or manually deriving the resistor and capacitor values themselves, designers can automatically calculate and assign values to the termination by making use of the powerful Terminator Wizard. When the analysis is complete the simulated results are easily stored for downstream design reviews or documentation purposes.

Integrated Digital, Analog, and Mixed Signal Design and Simulation

Also provided is a complete digital, analog and mixed signal simulation environment tailored for today's designs. Based on the principle that the simulation schematic equals PCB schematic, the single environment for circuit design and simulation enables an easy-to-use simulation process tightly integrated into the Xpedition and PADS PCB flows.

Simulation and Setup made Easy

A specific Simulation Toolbar and dialogs guide the designer through the entire simulation process making it very easy and intuitive to setup, simulate and analyze.

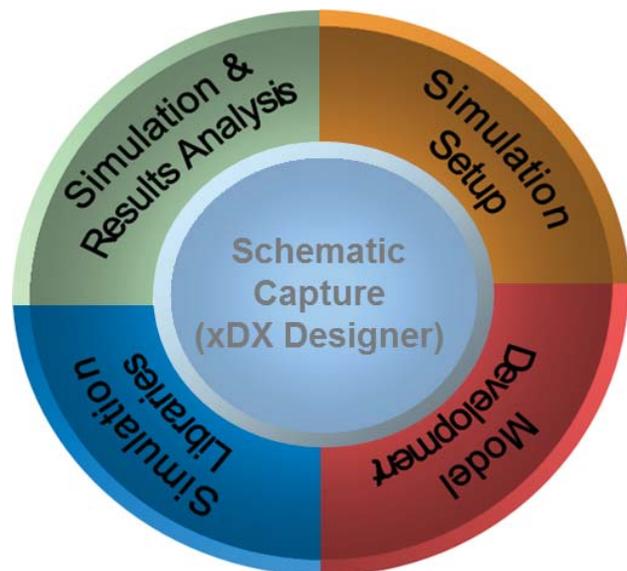
Other powerful and highly productive capabilities include:

- Drag-and-drop symbol creation
- Simulation model properties

- Pin to port mapping
- Reduce number of required properties
- Library manager integration
- Symbol editor integration
- Source dialog
- No probes required

Scalable for Complex Simulations

The environment provides a completely scalable simulation solution with a choice of simulation engines depending on circuit modeling and complexity:



Complete simulation environment,

- HyperLynx Analog – included as standard and UC Berkeley SPICE 2G.6 compatible
- Choice of Simulation Engines
 - Eldo™ - optional
 - ADMS: Full mixed-signal simulation (optional)
 - Verilog-A
 - Questa ADMS™ (VHDL-AMS)

The integrated HyperLynx Analog simulation environment simplifies the simulation of analog circuits, breaks down traditional barriers to simulation and can handle all of your digital, analog and mixed signal designs

FPGA/PCB I/O Optimization

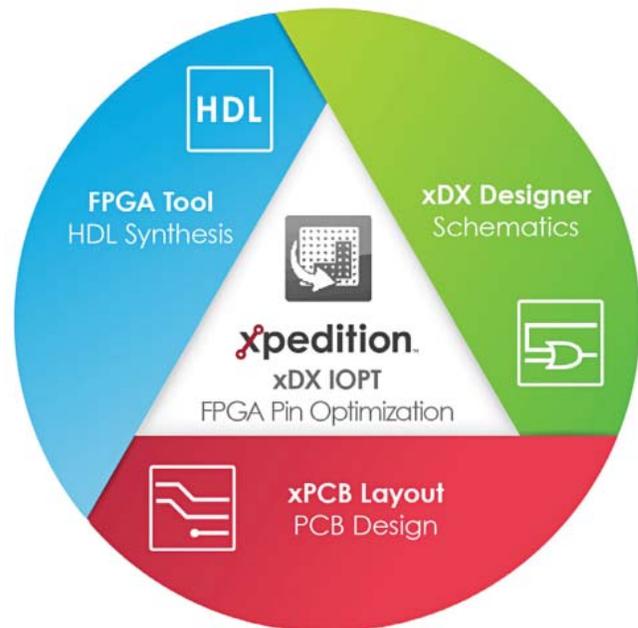
The xDX Designer cockpit also provides an extensive set of functionality via xDX IOPT to ease the FPGA-on-board integration process.

Aimed at the schematic and PCB engineer, xDX IOPT is the interface between the HDL design environment and the physical implementation on the PCB, significantly reducing both time-to-market and manufacturing costs.

PCB Flow Integration

Tight integration with the Xpedition Enterprise design flow allows creating or optimizing the FPGA at any stage of the project. Schematic, PCB layout and FPGA databases are kept in sync to control the project's design data flow.

In addition, schematic users can decide when the FPGA data is to be transferred to the PCB design. Before placement or routing is started on the PCB, users can begin floor planning, which can be exported to the Xpedition PCB Layout tool. The FPGA parts are managed at either the project or the enterprise library level.



For the latest product information, call us or visit: www.mentor.com/pcb

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