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## System Design — from Concept to Manufacturing

The Xpedition® Enterprise flow provides a clean, integrated design system from concept through manufacturing handoff. Tools are available for every aspect from system definition and simulation to schematic entry, constraint definition, layout, verification, Design for Manufacturability, through design data packaging for handoff to PCB fabrication.

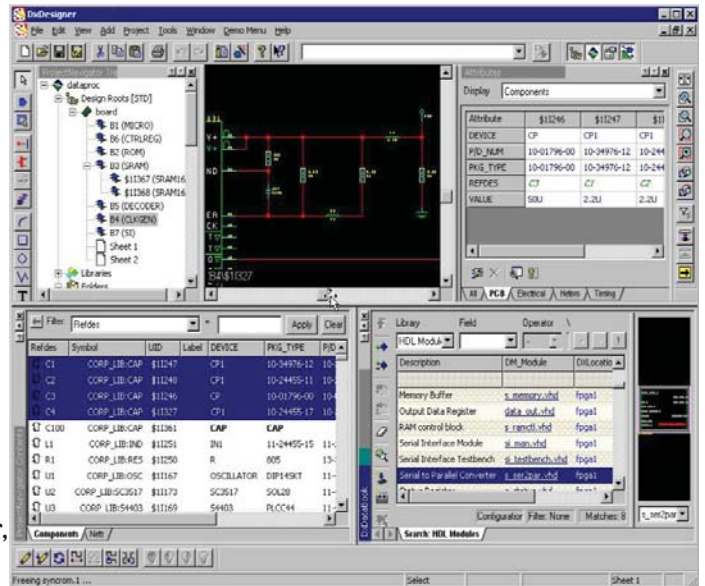
### Tightly Integrated Flow

The tightly integrated design environment of Xpedition, plus its industry-unique technologies and its ability to meet the needs of mid-sized to large electronics companies really sets it apart from the competition. It features a common database and user interface, with rules that eliminate the burden of managing multiple tools to complete a design.

The electrical and manufacturing constraint management system, coupled with its design data and library management provides

support for local or globally dispersed design teams to leverage their resources and reduce design cycle times. Data integrity is constantly maintained — from concept to manufacturing. Xpedition is integrated with a library and data management system and constraint manager, providing a central infrastructure for component libraries, design data versioning and management, design reuse, entry and management of high speed and manufacturing rules, and integration with corporate PLM systems.

Once the design is complete, integration with manufacturing output tools ensures that the integrity of the design is maintained.



Xpedition's tightly-integrated environment provides a complete solution for design creation, definition, and reuse.

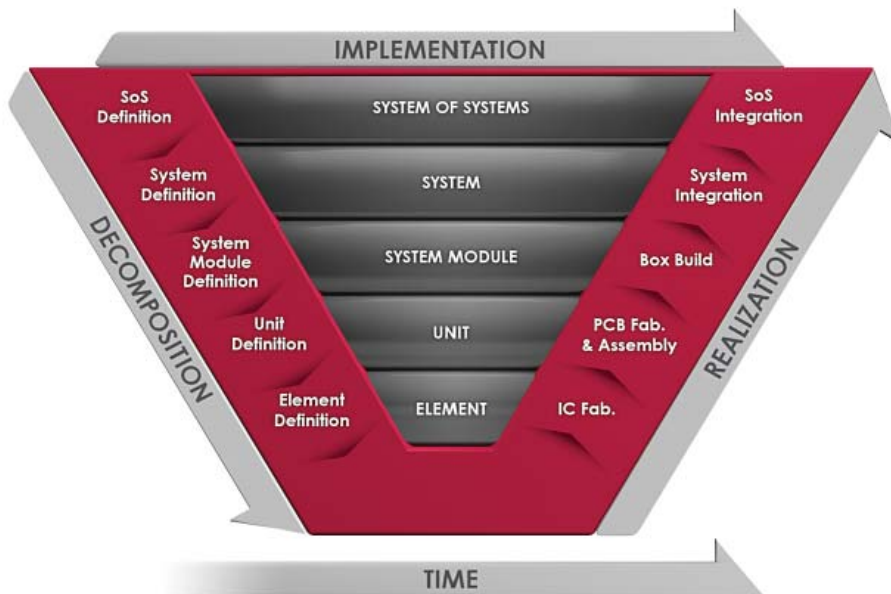
### Industry-unique Technologies

While tight integration provides a seamless environment to support the PCB systems design team, Xpedition has extended beyond the classical definition of a PCB design solution and contains many industry-unique technologies. These technologies address the most advanced business needs of an electronics company, enabling the development team to deliver a more competitive product to market faster and at reduced cost. These unique technologies fall into three categories: concurrent (parallel vs. serial) product development processes; use and analysis of the most advanced IC and PCB fabrication technologies; and, collaboration between the PCB designer and other disciplines in the product development process.

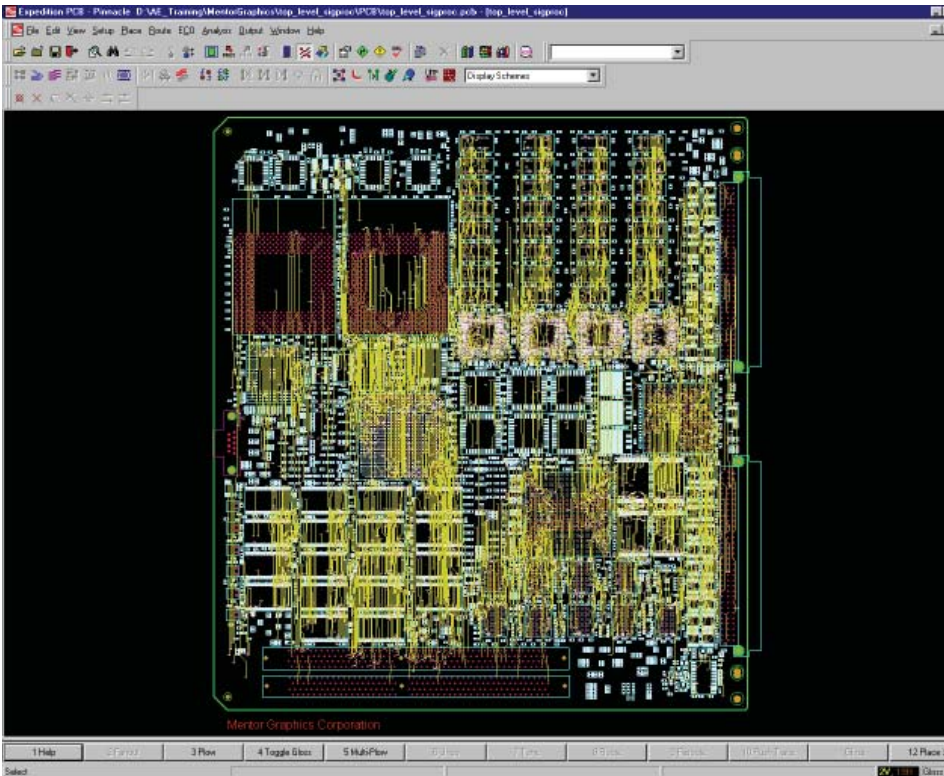
## System Definition

### Design Entry

Xpedition provides a complete solution for design creation, definition and reuse. It provides everything needed for circuit design and simulation, component selection and library management, signal integrity planning, project management and team-based



The Xpedition flow provides tools that address many areas of product design with a familiar interface and common database, facilitating new product design.



*Xpedition is simply the most productive solution available for the creation of dense, difficult, high technology PCB designs.*

design. With the schematic designer, multiple engineers can work on the same design concurrently without a classical split and re-join process. Changes made by one engineer are immediately reflected in the master database being viewed by the team so interfaces between the schematic sheets are kept in synchronization. In addition to classical schematic symbols, users can also employ spreadsheet input of component and interconnect data. This is especially important to accommodate very-high-pin-count packages, where a schematic symbol would occupy several pages.

The schematic designer is also integrated with product life cycle management systems, making design data, PDF schematics, and BOMs available throughout the company. It also has a centralized, Internet-based library so only one version of the corporate library needs to be maintained.

### FPGA-PCB Design Collaboration

To help with the growing demands of FPGA and PCB design, the FPGA I/O optimizer is a fast and efficient solution for assigning FPGA I/O-to-device pins in the PCB layout. The FPGA and PCB design flows are integrated to provide top-down concurrent design of the FPGA packages and the PCB, reducing the design cycle time and optimizing system-level performance.

By maintaining a library of parts from major FPGA vendors, the optimizer supplies all of the important information about each pin of the selected device. Users then choose to assign all of the signals to pins on the device or only those signals deemed critical to the PCB design. They can also assign I/O standards for critical signals. This way, the pinout of single or multiple FPGAs can be optimized prior to PCB layout to insure the best system performance, reducing PCB routing congestion and design

cycle time. Need to swap pins on the PCB to further improve the layout? The FPGA optimizer knows which pins are swappable and which are not. It also maintains the consistency between the FPGA and PCB flows by acting as a data management tool, monitoring each flow and managing any changes that occur. Pin swaps carried out on the PCB are picked up by the optimizer and the necessary FPGA files updated. It then generates FPGA place and route constraints, based on the HDL design and pin I/O assignment process, and creates the necessary symbols, schematics and hierarchical associations based on the “post route” pin data.

### Constraint Definition

Xpedition understands and follows an extensive set of high speed and manufacturing constraints (rules). These constraints are set either by engineer direct entry or by interfacing from pre-layout high speed analysis and are obeyed throughout the layout and verification steps to insure correct by design results.

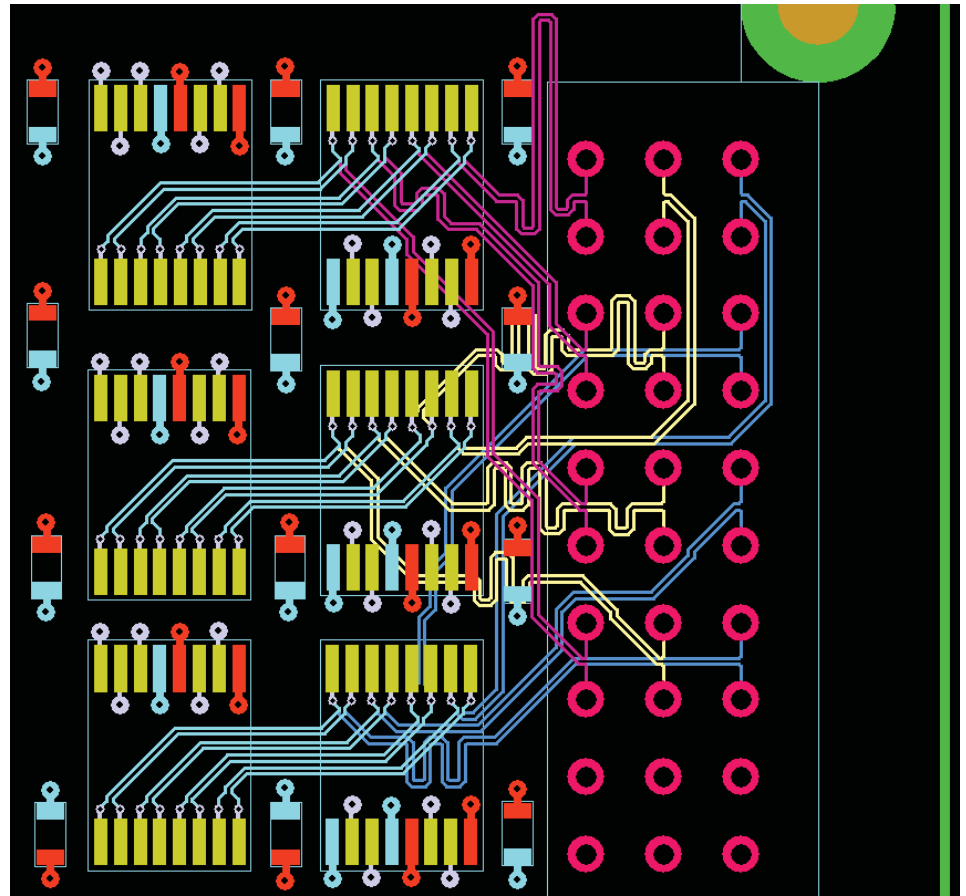
The constraint manager provides a fully integrated, constraint-driven design methodology that reduces design costs and time-to-market by automating design rules communication and eliminating unnecessary PCB prototypes and re-spins. And, like the schematic designer, multiple engineers can input and edit constraints concurrently without a divide and re-join methodology that can be error prone and time consuming. Edits are viewed by the team as they are made, in real time. The constraint manager provides common constraint entry for manufacturing and electrical and physical high-speed rules. The constraint manager has an easy-to-use spread-sheet-like GUI guided by the design database with cross probing to the schematic and layout.



- Rules are preserved on net renames, connectivity additions/removals, pin and/or gate swaps, and stackup changes.
- The GUI offers easy differential pair creation, parallelism rules entry and pin-pair creation.
- Hierarchical constraint entry enables simple assignment of complex topologies with filtering and sorting.

## PCB Layout

Xpedition is the most powerful physical-layout solution in the industry. By combining ease-of-use with advanced functionality, Xpedition offers designers the leading technology to create today's most complex designs. It includes interactive and customizable multi-pass auto-routing controls for design challenges, such as differential pair routing, net tuning, manufacturing optimization and HDI/microvia and buildup technology.



*Routing and editing differential pairs with Xpedition's layout tool is accomplished with speed and ease that will change your view of high-speed design.*

## The Physical Layout Technology Leader in PCB Design

Xpedition's placement and routing technology represents a revolutionary step forward for PCB design. The power of industry-leading auto-routing technology is combined with interactive editing capabilities to produce a single, powerful and easy-to-use design environment. This environment eliminates the burdens of jumping between tools to get the job done and managing differences between the constraints on the auto-router and on interactive editing. Xpedition provides greater control than ever before, easily switching between automatic and manual editing as needed. From simple tasks, such as defining board areas, to complex procedures that involve maintaining high-speed signal conditions, all objectives are accomplished with the system and the designer working together in real time. The net result of Xpedition's technology is reduced

design times, increased productivity and unmatched design quality.

### Auto and Interactive Routing

- A single, integrated, place-and-route editing environment that reduces total design time and increases productivity.
- All physical rules and high speed rules are maintained.
- Correct-by-construction design that produces high-quality results with clean-up time eliminated.
- Shape-based, true 45° routing and advanced any angle push/shove for the most challenging BGA patterns..
- The most advanced auto-routing technology ever. Stop and start the auto-router at any time: all results will be correct-by-construction.

- Dynamic clean-up of traces through the reduction of segments, prevention of acute angles, and application of pad entry rules.

### Dynamic Area Fills

Xpedition automatically clears area fills around traces, vias and pads as the board is edited. Dynamic area fills are so fast, it allows users to keep their area fills turned on while they are doing all necessary edits. Moving a via pushes and shoves other vias, traces and area fills and connectivity is automatically maintained.

### Rules By Area

The rules-by-area function greatly improves routing around BGAs and other fine-pitched parts. Rule areas represent complete rule sets that are obeyed by online and batch DRC and in interactive and automatic routing. Rule areas may be defined by layer and can be

assigned to any polygon, rectangle or circle. Trace widths and clearances automatically change when within the rule area. Designers may also change via sizes and spans in a rule area to maximize route completion.

### **Multiplow with Variable Via Patterns**

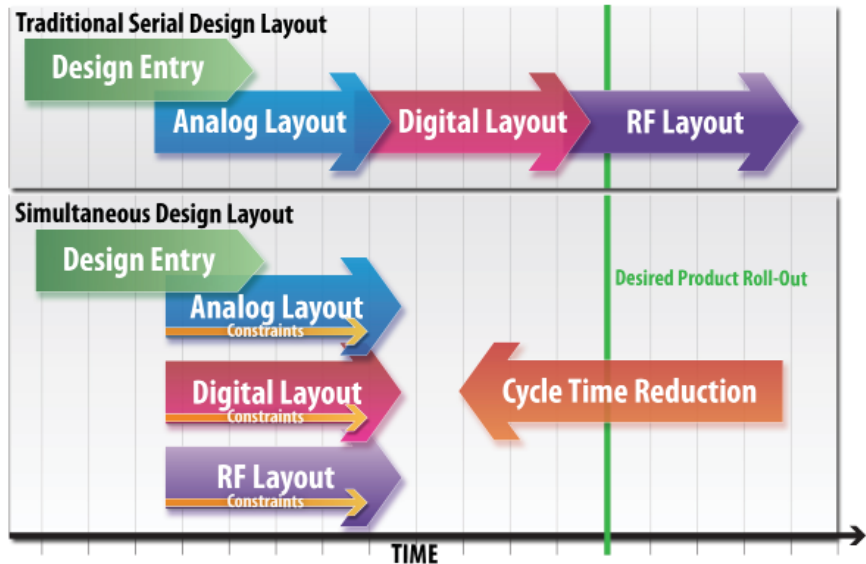
Xpedition's multiplow functionality allows designers to simultaneously route multiple nets, including differential pairs, with true 45° routing with any angle as well as offset angle routing. It can even handle routing through areas of staggered pins. Traces being routed push and shove the other vias and traces and automatically clear area fills as needed. Changes can be easily made to a variety of selectable via patterns at the touch of a button, allowing enhanced flexibility for routing into dense areas of a design.

### **High-Speed Layout**

Designers must increasingly manage signal quality to achieve system performance and reduce prototype iterations. High-speed design with Xpedition is an integrated part of the design environment. Dynamic DRC of high-speed rules, automated tuning for the most complex high-speed constraint definitions, and dynamic tuning keeps nets within tune. Its spacer technology helps to manage crosstalk.

### **Net Tuning**

While routing interactively, graphic tuning aids are displayed for guidance. Nets modified out-of-tune during edits are automatically re-tuned. The hazards dialog box dynamically updates as users edit nets, providing instant feedback to their constraints. Nets can also be tuned automatically within an auto-route pass. Tuned nets are automatically maintained as the designs are completed.



*Concurrent team design technology allows designers to work simultaneously on the same PCB, accelerating the design process.*

### **Differential Pair Routing**

Routing and editing differential pairs with Xpedition is accomplished with speed and ease that changes the view of high-speed design. Impedances can be easily controlled by layer and pair spacing rules can be established by both layer and net class. If one trace is edited, the other trace in the pair automatically moves with it. Adjacent layer differential pair routing capabilities add another valuable option for routing critical signals on a dense PCB.

### **Dynamic Hazard Review**

Design hazards are dynamically displayed and may be individually selected and colored for easy identification. When a hazard is fixed, it is dynamically removed from the hazard list.

### **Simultaneous Design**

Leveraging a revolutionary, patented, and exciting technology that enables multiple PCB designers, locally or globally dispersed, to simultaneously work on a single design database over a LAN or WAN provides unprecedented design efficiency. Unlike traditional team design methodologies that employ a split-and-join approach to design collaboration, concurrent team

design requires no physical partitioning and every designer sees all other client edits in real time. Because no further training or complex setup is required, designers can be brought in at any time and from anywhere to collaborate on time-critical projects, dramatically shortening design time. Ideal for large, complex designs or when specialists work on their specialty in a mixed-signal environment.

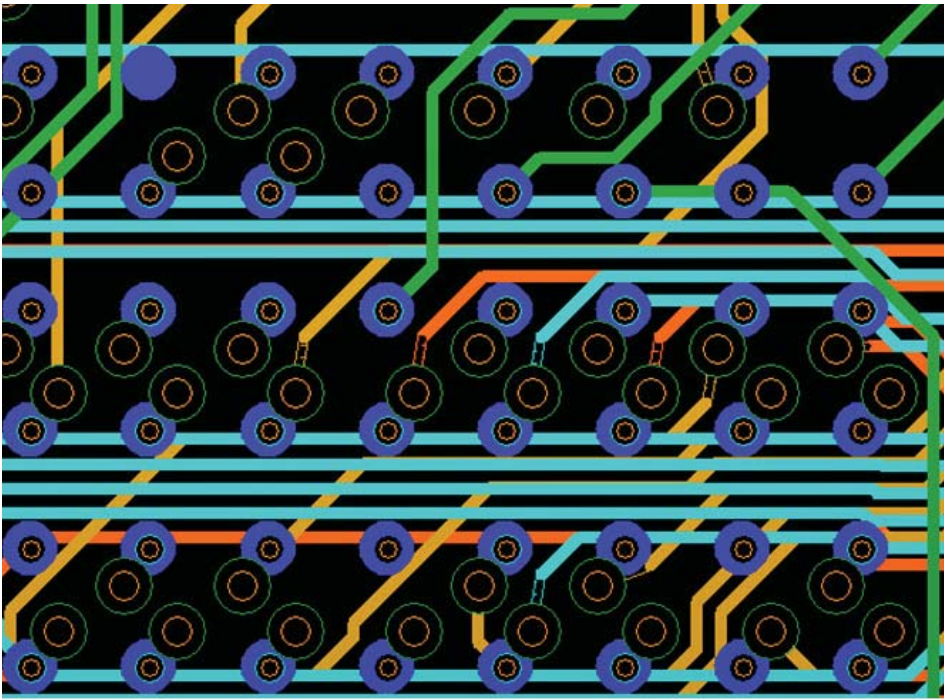
### **Multi-user Auto-routing**

The same technology that enables simultaneous design on the same database by multiple designers enables multi-processor auto-routing. By executing the auto-routing on up to 15 processor clients on a LAN or WAN network, users can obtain up to a 10x improvement in elapsed times. For very large, highly constrained boards, this can reduce the times from days to hours. The result is not only a decrease in design times but the opportunity to run multiple scenarios of placements and constraints and pick the the most cost-effective one.

### **Bus Routing**

Auto-routing is rarely used on dense, highly bus-structured PCBs, as manual routing can produce





*Using the built-in HDI support in Xpedition, much more efficient fanouts can be designed, enabling much smaller footprints and cost savings.*

denser, more manufacturable and aesthetic results. However, manual routing can be very time consuming and tedious.

Skillful designers or engineers determine the topology of the buses and their assigned planes to meet high-speed constraints. Xpedition has unique technology that combines the skill of the designer and engineer with the speed of auto-routing, eliminating the tedium, instead focusing on producing a better design. Topology Planner provides an interactive method of defining the topologies of buses, assigning them to planes and specifying many specialized rules. This plan is saved with the design data and can be modified. The topology router can then be executed to auto-route the interconnects following the plan, eliminating tedious trace digitizing. The results mimic those of a skilled designer, yet significantly reduce design cycle times and improve productivity.

### **Embedded Passive Design**

As ICs and FPGAs increase in speed and density, they require more passive components

(resistors and capacitors) — some may need several hundred. Implementing these as embedded components versus discrete SMDs can significantly reduce board sizes and improve performance.

Xpedition provides a complete solution: trade-off tools decide which components to implement in embedded versus discrete based on board size and cost, passive material choices, automatic synthesis driven by material supplier's libraries, and full manufacturing data generation. The result is automation of a task that could take weeks of manual effort.

### **Advanced Interconnect Routing**

The challenges and solutions of advanced interconnect are prevalent today with BGA, CSP, COB and DCA packages increasing board density. Build-up and microvia structures used in these board designs further complicate routing.

Xpedition offers the leading technology for advanced interconnect designs. Breakout and Escape technology allows rapid

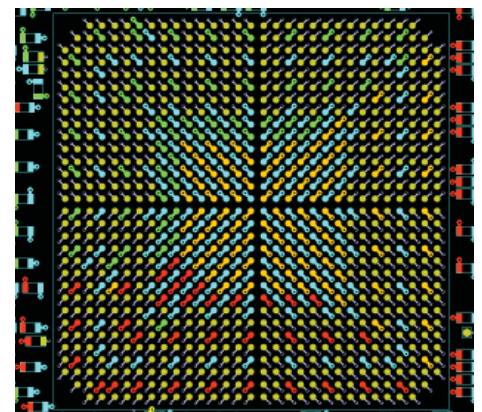
routing of the highest pin-count packages with very fine pitch pins/balls. Both stacked and staggered via definitions can be defined, providing control over the via structures that are placed.

Moving beyond traditional laminate layer pairing facilitates the design of build-up structures on laminate to enable escape patterns from dense, high-pin-count devices. Build-up areas typically have a smaller clearance than the laminate beneath them.

Delay values and clearances per via span can be established to address these issues. Additionally, Xpedition features true 45 degree routing and advanced any angle push/shove for the most challenging BGA patterns.

### **High-density BGA Fanout**

Connecting to today's advanced packages can be a time consuming task for the designer. Industry unique technology in Xpedition enables automatic fanout of high pin-count and density BGAs. Following Mentor published design guidelines, the user can define the fanout pattern using HDI/microvia layers and develop the pattern in seconds. Then, in the context of the other PCB components, define and automatically produce a breakout that connects to the rest of the PCB. Reducing to minutes what used to take days of designer time.



*Complex fanout patterns can be created in seconds with Xpedition.*

## RF Circuit Design

With the increase of wireless technology, more PCB designs mix RF circuitry with their analog and digital interconnect. Typically, designing these boards required two completely different tools and libraries. Mentor's leading technology enables RF circuit design in the Xpedition environment including schematic entry, synthesis of RF parts using the same libraries as the RF simulation providers, manipulation and editing RF circuitry, and direct interface to RF simulators from suppliers like Agilent and AWR. The result is a highly productive process that integrates the design and design team, eliminates duplication and synchronization of libraries, and capitalizes on the strengths of Mentor's PCB design and the RF simulator suppliers' technology.

## Analysis and Verification

### Signal Integrity, Timing Analysis and EMI

With the Xpedition flow, signal integrity and electromagnetic interference (EMI) issues can be addressed and corrected

throughout the design process rather than just at the end. Driven by constraints, this ensures that designs are correct the first time, effectively reducing design iterations and facilitating optimum system performance.

HyperLynx® provides pre- and post-layout signal integrity, crosstalk and EMC analysis for traditional high-speed interconnects, as well as the emerging SERDES and DDR2/3 technologies, as well as advanced SERDES and DDRx protocols. HyperLynx's easy-to-learn analysis environment makes it an every-desktop standard for Xpedition. Higher-frequency designs and government regulations place increasing importance on EMI control. This normally required a prototype board, testing in a shielded chamber and re-design.

### Power Integrity

With today's lower and multiple voltage ICs, power and ground is no longer easy to design and analyze. PCBs can contain as many as 30 power distribution networks jig-sawed into the PCB layers. These networks must be analyzed for DC voltage drop (sufficient power to all IC pins), current density (too much current

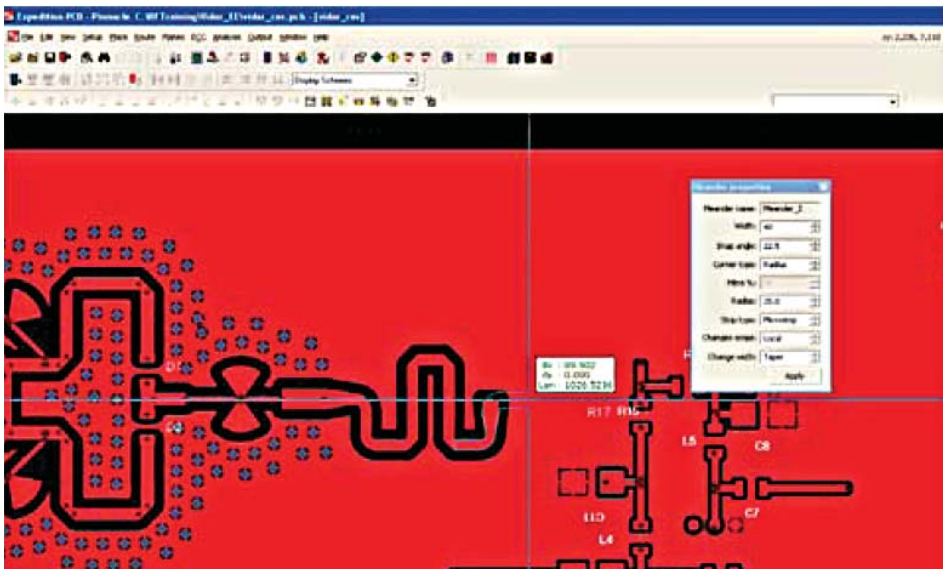
through a narrow part of the network), and AC (is the power clean). HyperLynx PI (Power Integrity) provides the engineer and designer with pre- and post-layout analysis of complex power distribution networks to insure proper operation and high reliability of the PCB.

### Thermal Analysis

As products get faster and smaller, thermal management issues increase. HyperLynx Thermal, FloTHERM®, and FloEFD® provide thermal analysis capabilities for the PCB as well as the PCB(s) in the full product (enclosure, fans, heat sinks, etc.). Using these capabilities, the PCB designer can perform analysis on the PCB to determine good placement of the components. The mechanical designer of the enclosure can insert the PCB(s) into the complete product and analyze it to see if the heat will be dissipated properly. The result is a design that has higher reliability and can be manufactured without multiple prototypes or re-spins.

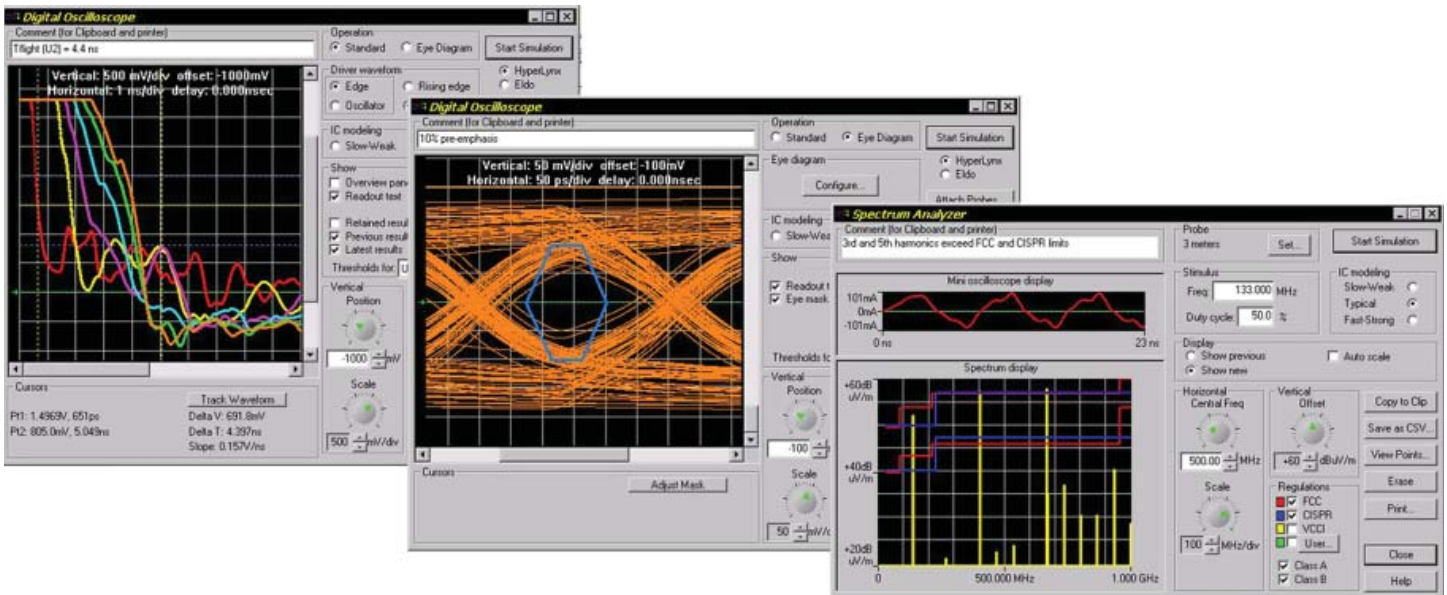
### Mixed Signal Verification

HyperLynx Analog™ verifies analog and mixed analog/digital designs at the system or board level. It is tightly integrated into the schematic designer and combines ease-of-use with powerful simulation, stimuli preparation, and complex circuit analysis and verification. ModelSim® is the world's most popular and widely used VHDL and mixed-VHDL/Verilog simulator and the fastest-growing Verilog simulator. ModelSim products are unique, using technology such as Optimized Direct Compile for faster compile times and simulation performance, Single Kernel Simulation (SKS) and Tcl/Tk for greater openness and faster debugging. These exclusive ModelSim, innovations result in leading compiler/simulator performance, complete



*Xpedition understands RF circuitry, allowing wireless components to be designed onto digital and/or analog boards.*





*HyperLynx enables powerful, easy-to-use simulation and analysis for signal integrity, power integrity, thermal, and design rule checking. Wizards allow rapid setup of simulation parameters and execution.*

freedom to mix VHDL and Verilog and the unmatched customization.

### Design Rule Checking

HyperLynx DRC is a rule checking tool that is fully customizable. It verifies complex design rules that are not easily simulated, such as rules for EMI/EMC. With 19 standard design rule checks for items such as traces crossing splits, reference plane changes, shielding, and via checks, you can quickly and easily pinpoint trouble spots on your board that can cause issues with EMI/EMC, signal integrity, and power integrity.

HyperLynx DRC accesses database objects through the automation object model (AOM), and allows advanced geometrical operations on these objects. This gives you unique access to the design database and allows development many types of DRCs. With support for VBScript and JavaScript, as well as thorough documentation of the AOM and DRC coding standards, and a built-in script debugging environment, users can be writing your own DRCs immediately.

### Multi-disciplined Collaboration

Developing an electronic product requires more than the design of the PCB. The mechanical enclosure must be designed. Procurement, test and manufacturing must be involved throughout the design process to insure that the product can reach volume production in time to hit the market window. Xpedition provides the ability for these disciplines to collaborate during the product development process.

### ECAD-MCAD Collaboration

In the past, communication between the electrical designer and the mechanical designer was performed via paper or through mass data transfers. Xpedition provides 3D viewing capability for the PCB designer to insert the PCB into the enclosure and identify gross errors such as interference of components with the enclosure. But true collaboration goes beyond 3D viewing. Xpedition also provides the ability for bidirectional, electronic communication of incremental change proposals. Using this ECAD-MCAD collaboration, either discipline can propose a change in

their domain and communicate that proposal to the other. The proposal can then be analyzed, rejected, accepted, or counter-proposed. This digital process continues until both disciplines are satisfied at which point the change is reflected in both databases.

### PCB Designer – Supply Chain Collaboration

Late changes in the PCB design can negatively affect the ability for procurement, manufacturing and test to deliver volume production targets. Xpedition enables the PCB designer to propose a change and electronically communicate that proposal to the rest of the supply chain organizations. The design review tool enables these organizations to view the proposed change and communicate back to the designer through mark-ups and red lines whether this change is acceptable. This negotiation process continues until an acceptable solution is reached.

### DFM Verification

The creation of manufacturing data and the distribution to production sites introduces challenges at a point in the design process where errors can become



very costly, in terms of time and money.

The constraint manager contains manufacturing rules that are dynamically checked during the design process. In addition, Xpedition is tightly integrated with Valor NPI, providing access to the industry-premier solution for DFM validation, leveraging the same constraints used for final verification on the manufacturing side.

Manufacturing documentation and outputs can be created directly within the layout environment, so any last-minute layout changes are automatically synced. Automated and customizable creation and distribution of manufacturing data results in increased quality, accuracy and design throughput. Data can be output in ODB++, ensuring that all manufacturing data is included and synchronized. Additional CAM formats including Gerber, ATE and AIS Drill are also supported.

### DFM Validation

Concurrent DFM verification with the Valor NPI product is the most efficient way to incorporate manufacturability into your PCB design process. Identify the opportunity for fabrication, assembly and test improvement during design, and avoid manufacturing-initiated Engineering Changes. You can even automate the intervals for DFM verification and review results in a timely manner so the design flow is streamlined and efficient. If an error is identified, a single click takes you to the location on your PCB design so that you can remedy the issue.

### Comprehensive Analysis

Your DFM process is only as good as the verification tools you use. Today's miniaturized, high-layer count designs cannot be reliably reviewed by manual means. The DFM validation software analyzes your PCB design with more than:

- 275 Fabrication checks
- 250 Assembly checks
- 100 Advanced Substrate checks
- 40 Microvia checks
- 30 Panel checks

In addition, the DFM validation tool provides the ability to check your Netlist against the design data to assure there are no fatal errors within this critical step. It validates that your BOM matches the design, and that all components in your Approved Vendors List (AVL) are an acceptable physical match.

### Design Center Customization

Every design center and every technology type have their own unique requirements with respect to manufacturability.

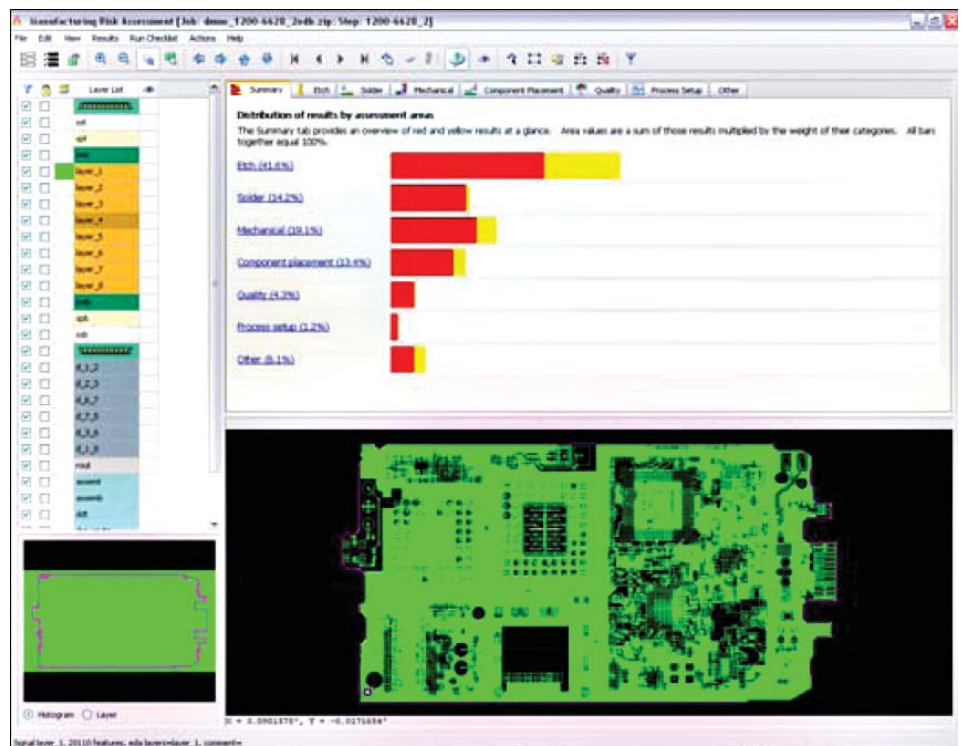
From data attribution to manufacturing rules values, you need to be able to run DFM at the highest level of automation. The DFM validation tool uses a Design Center concept to allow customization of the DFM process

flow, attribute mapping, component classification, and, the set-up and management of manufacturing rules files. Using a hierarchical approach, you create a master rules model using constants and variables that drive derivative rules models. This greatly reduces the support requirements for your DFM environment.

It even provides a default master set compliant with the IPC-7351 standard.

### Understand the Manufacturing Risk

The DFM validation tool not only identifies where your PCB design is in hard violation of your supplier's manufacturing capabilities, it also shows where yield or field failure issues may occur by using color severity indicators of red, yellow, and green. DFM validation further categorizes and prioritizes the issues so that you may easily resolve the most critical first. The weight assigned to each check is user-definable, enabling you to apply criteria to how the results are prioritized. After all, your



DFM issues are summarized and ranked by severity, based on weighting set by the user in the tool.

technology and suppliers' processes are likely different than another company's processes.

### **Prepare for Fabrication**

Manufacturing and fabrication have always been an integral part of PCB design. Previously, designers used multiple applications to create schematics, layouts and prepare for manufacturing. To make the process easier, Xpedition integrates the fabrication preparation environment for manufacturing data creation, generation and verification. Fabrication preparation enables designers to control their fabrication data at either the board or panel level, ensuring design and manufacturing data integrity.

Fabrication preparation provides a standalone panel creation and editing environment for creating manufacturing data at the panel level, using a panel design database. It also provides additional board level functionality, including detailed data views, searchable PDF output, copper balancing, data outputs and Gerber In/Drill In capabilities.

### **Automation**

Automation provides customization and extensibility within the design and layout products, allowing the addition of custom functionality, the automation of repetitive tasks, and the ability to tailor the flow to customer-specific use-cases and optimize the flow for specialized processes. The use of a wide range of industry-standard languages (VBscript, Jscript, TCL, Java, VB6, C++, C#, VB.NET...) minimizes the start-up time for company programmers

and facilitates script reuse. The result of automation is to reduce errors, increase productivity, increase the performance, quality, and reliability of the design, decrease the cost of the design, and decrease time to market (and time to profit).

### **Intellectual Property Management**

The data management system brings the electronic design process to the supply chain, and brings the supply chain to the designer's desktop. It ensures complete data consistency, accuracy and availability throughout the design process. Plus, it consolidates multiple data systems, for collaboration and life cycle management across multiple team members, disciplines and sites.

It does this by integrating design data management with component information so that corporate component procurement policies (approved parts, preferred vendors) are easily available on the desktop. This helps designers make optimum component choices and manage parts lists during the design process so they can be released as accurate BOM's meeting corporate policies for cost, reliability and regulatory compliance.

At the end of the project, it manages the process so that accurate product documentation can be released to enterprise manufacturing, PLM and ERP systems, and supply chain management systems.

### **Design Reuse**

Create and store reusable blocks of circuitry, including schematic, as well as PCB placement and routing data, in a central library. These blocks can then be placed and modified in the same design or multiple designs now and in the future. Design reuse automates this process and manages the design data to ensure error-free databases and reduce the overall PCB design cycle time by not having to re-design the same circuit. Layout data can also be easily cut/pasted within a design and into other designs, enabling informal reuse of sections of a design.

### **Variant Management**

A variant manager handles the creation of multiple product configurations from a single design database. The variant manager's single-point ECO management minimizes errors, reduces costs, improves design quality and enhances production efficiency.

### **Support, Education and Consulting**

Mentor Graphics offers a full range of services to drive your productivity and success with the Xpedition flow tools. Customer Support offers award-winning technical assistance, innovative electronic support and high-quality product enhancements. Education Services offers classroom and online training to help you assimilate new tools and technologies into your design environment. Finally, Mentor Consulting is always ready to provide focused expertise in tough design areas.





Mark Forbes Photo

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